REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1, 3 through 8, 10, 15, 16, 19 through 22, and 43 through 48 remain now in this case. Claim 48 is amended.

Claim 48 is amended for clarity, specifically to correct an obvious error in the preamble; no change in the scope of this claim is intended or results from this amendment to the claim.

Claims 1, 3 through 6, 8 through 10, and 43 through 45 were again rejected under §102 as anticipated by the Achiwa et al. reference[1]. Claim 7 was again rejected under §103 as unpatentable over the Achiwa et al. reference in view of the in view of the Kramer reference.[2]

Applicants respectfully traverse the rejection of claim 1 and its dependent claims, on the grounds that the basis of the rejection is in error. The nature of this error is especially evident considering that the rejection is inconsistent with the interpretation of the Achiwa et al. reference now being propounded by the Examiner.

In response to Applicants' arguments in the Submission Under Rule 114, the Examiner has now made a direct correspondence between elements of the non-volatile memory of the Achiwa et al. reference, and the memory system elements upon which the method of claim 1 operates.[3] This correspondence is as follows:

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[1] U.S. Patent No. 5,737,742, issued April 7, 1998 to Achiwa et al.

[2] U.S. Patent No. 6,182,239 B1, issued January 30, 2001 to Kramer.

[3] Office Action of March 22, 2007, page 3.

Achiwa et al.	Claim 1
"plurality of individually erasable physical blocks"[4]	"plurality of erase units"
"plurality of sectors within a physical block"[5]	"plurality of programming units"
"memory cell"[6]	"non-volatile memory cells"

In other words, the Examiner finds that the Achiwa et al. reference teaches a non-volatile memory having a plurality of individual erasable physical blocks, each including a plurality of sectors within each physical block, each sector including a plurality of memory cells, and that this memory corresponds to a non-volatile memory having a plurality of erase units, each erase unit including a plurality of programming units, each programming unit comprising a plurality of non-volatile memory cells, as recited in claim 1. Applicants do not disagree with this characterization, and find it to be a reasonable interpretation of the Achiwa et al. reference.

However, the Examiner maintains the original basis of rejection, including a finding that the Achiwa et al. reference teaches the step of grouping programming units within the first erase unit into a plurality of groups of programming units, arranged in a sequence, by way of its "second classifying section for classifying the physical blocks into a plurality of groups on the basis of the respective erasure counts of the physical blocks".[7] This assertion is inconsistent with the new characterization of the Achiwa et al. reference presented by the Examiner in response to the Submission Under Rule 114. As noted above, the Examiner considers the sectors within a physical block, taught by Achiwa et al., to correspond to the programming units of claim 1. This is inconsistent with the Examiner's assertion that "classifying *the physical blocks* into a plurality of groups on the basis of the respective erasure counts *of the physical blocks*" meets the claim step of grouping programming units *within* a first physical block into a plurality of groups.

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[4] *Id.*, *citing* Achiwa et al., *supra,* Abstract, and Figure 2 (element 1110).

[5] *Id.*, *citing* Achiwa et al., *supra,* column 1, lines 60 through 65.

[6] *Id.*, *citing* Achiwa et al., *supra,* column 1, lines 17 and 18.

[7] Office Action, *supra,* page 6, *citing* Achiwa et al., *supra,* abstract, Figures 3 and 7 (emphasis in original removed).

The Examiner cannot have it both ways. If the Examiner considers the physical blocks of Achiwa et al. to correspond to the programming units of the claims, for purposes of meeting the grouping step, then the physical blocks of Achiwa et al. cannot correspond to the erase units of claim 1, as asserted in response to the Submission Under Rule 114. Conversely, if the Examiner considers the physical blocks of Achiwa et al. to correspond to the erase units of the claims,[8] as asserted in response to the Submission Under Rule 114, then the grouping of the physical blocks cannot correspond to the grouping of programming units within the first erase unit into a plurality of groups, as required by claim 1. The basis of the §102 rejection, as stated in the Office Action, is therefore in error, because it is inconsistent with the Examiner's own interpretation of the reference.

Applicants further submit that the Achiwa et al. reference in fact does not teach the grouping of programming units within an erase unit into a plurality of groups. If one accepts the Examiner's characterization of the Achiwa et al. reference summarized above, in which the sectors within a physical block of the Achiwa et al. reference correspond to the programming units recited in claim 1, then the Achiwa et al. reference must teach the grouping of its sectors, within a physical block, into a plurality of groups of sectors within that physical block, in order to anticipate claim 1. The Achiwa et al. reference contains no such teaching regarding the grouping of sectors within a physical block into a plurality of groups of sectors.

Applicants therefore submit that the Achiwa et al. reference in fact fails to disclose the grouping step of claim 1. And because the reference fails to disclose a plurality of groups of programming units within an erase unit into a plurality of groups of programming units, much less arranged in a sequence, Applicants submit that the Achiwa et al. reference therefore necessarily fails to meet the writing steps of independent claim 1, each of which refer to writing contents of a logical sub-unit into a programming unit in a specified one of these groups of programming units.

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[8] And thus the sectors within a physical block, of Achiwa et al., to correspond to the programming units of the claims.

For these reasons, Applicants submit that the §102 rejection of claim 1 and its dependent claims is in error, and submit that these claims are in fact novel over the Achiwa et al. reference, properly interpreted.

Applicants also maintain their argument that, because none of the other prior art of record in this case, including the Kramer reference asserted against claim 7, disclose or suggest the grouping of programming units, as required by claim 1, the combined teachings of the prior art fall short of claim 1 and its dependent claims. Especially considering the important advantages provided by claim 1 and its dependent claims in enabling efficient out-of-sequence write operations within a given physical block (erase unit), even in a flash memory of a type (*e.g.,* NAND memory) in which out-of-sequence write operations are prohibited, and considering that these advantages stem directly from the difference between the claims and the prior art, Applicants submit that claim 1 and its dependent claims are not only novel, but patentably distinct over the prior art of record in this case.

Independent claim 22 and its dependent claims 15, 16, 19 through 21, and 46 through 48 were again rejected under §102 as anticipated by the Achiwa et al. reference, on the same grounds as discussed above relative to claim 1.[9] Claim 21 was again rejected under §103 on similar grounds as claim 7.

Applicants also traverse the rejection of claim 22 and its dependent claims, on the grounds that the rejection as stated is in error, and that in fact claim 22 and its dependent claims are novel and inventive over the prior art, including the Achiwa et al. reference.

Again, Applicants do not disagree with the interpretation of the Achiwa et al. reference presented by the Examiner in response to the Submission Under Rule 114, and accept that this interpretation is a reasonable one. In short, the Examiner interpreted the physical blocks in the Achiwa et al. reference to correspond to the erase units of the non-volatile memory of claim 22, the sectors within the physical blocks in the Achiwa et al. reference to correspond to the programming units of the memory of claim 22, and the memory cells within the sectors in the Achiwa et al. reference to correspond to the memory cells of the programming units of claim 22.

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[9] Office Action, *supra*, page 10.

But the stated basis of the rejection of claim 22 is inconsistent with this interpretation of the Achiwa et al. reference. Specifically, as in the case of claim 1, the Examiner asserted that the "second classifying section for classifying the physical blocks into a plurality of groups on the basis of the respective erasure counts of the physical blocks", taught by the Achiwa et al. reference, teaches the plurality of groups of programming units within an erase unit, according to which the controlling means of claim 22 operates.[10] This is contrary to the Examiner's new interpretation of the reference, in which the physical blocks of Achiwa et al. are found to correspond to the *erase units* of the recited memory, and not to the *programming units* that are grouped into a plurality of groups within an erase unit, as claimed. If the new interpretation is followed, then the groups of physical blocks taught by Achiwa et al. cannot correspond to the groups of programming units, because the Achiwa et al. physical blocks correspond instead to the erase units of the claimed memory. Accordingly, Applicants submit that the §102 rejection of claim 22 and its dependent claims is in error, because the basis of rejection is contrary to the Examiner's own interpretation of the reference.

Furthermore, Applicants submit that the Achiwa et al. reference in fact does not teach the groups of programming units within erase units, as required by the memory of claim 22. Accepting the Examiner's reasonable interpretation of the reference, in which the sectors within a physical block correspond to programming units of claim 22, the Achiwa et al. reference contains no teaching or suggestion of the grouping of its sectors into groups within the physical block. Furthermore, since the reference fails to teach a plurality of groups of sectors (or other programming units) in a physical block, it necessarily fails to teach the other operations carried out by the controlling means of claim 22, including the writing of the contents of a logical sub-unit into programming units within specified groups of programming units in an erase unit.

For these reasons, Applicants submit that the system of claim 22 and its dependent claims is novel over the Achiwa et al. reference.

Applicants further submit that the groups of programming units within erase units, as required by claim 22, is also not taught by any of the prior art of record in this case, including the

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[10] Office Action, *supra,* page 6, *citing* Achiwa et al., *supra,* abstract, Figures 3 and 7 (emphasis in original removed).

Kramer reference asserted against dependent claim 21. Furthermore, considering the important advantages in enabling out-of-sequence writes in a flash memory that is not otherwise arranged to enable such out-of-sequence write operations, as provided in the system memory of claim 22 and resulting directly from the difference between the claims and the prior art, Applicants also submit that claim 22 and its dependent claims 15, 16, 19 through 21, and 46 through 48 are all patentably distinct over the prior art of record in this case.

For these reasons, Applicants respectfully submit that the claims now in this case are in condition for allowance. Reconsideration of this application is respectfully requested.

Respectfully submitted,

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